WHAT IS CLAIMED IS:

1. A memory component with built-in self test, comprising:

an input/output interface coupled to the memory array and having a loopback;

a controller to transmit input/output test data to the input/output interface, and to receive the input/output test data from the loopback of the input/output interface; and

a compare register to compare the input/output test data transmitted to the input/output interface with the input/output test data received from the input/output interface.

2. The memory component according to claim 1, wherein the memory component is a dynamic random access memory (DRAM).

3. The memory component according to claim 1, wherein the memory component is a buffer.

4. The memory component according to claim 3, wherein the buffer is an address and command buffer.

5. The memory component according to claim 3, wherein the buffer is a data buffer.

6. The memory component according to claim 3, wherein the buffer is an address and command and data buffer.

7. The memory component according to claim 1, wherein the compare register generates a test result based on the input/output test data transmitted to the input/output interface compared with the input/output test data received from the input/output interface.

8. The memory component according to claim 1, wherein the controller is adapted to transmit memory array test data to a memory array to store the test data therein, and to read the memory array test data from the memory array, and the compare register is adapted to compare the memory array test data transmitted to the memory array with the memory array test data read from the memory array.

9. A memory component with built-in self test, comprising:

a memory array;

an input/output interface coupled to the memory array and having a loopback;

a controller to transmit memory array test data to the memory array to store the memory array test data, and to read the memory array test data from the memory array; and

a compare register to compare the memory array test data transmitted to the memory array with the memory array test data read from the memory array.

10. The memory component according to claim 9, wherein the memory component is a dynamic random access memory (DRAM).

11. The memory component according to claim 9, wherein the memory component is a buffer.

12. The memory component according to claim 11, wherein the buffer is an address and command buffer.

13. The memory component according to claim 11, wherein the buffer is a data buffer.

14. The memory component according to claim 11, wherein the buffer is an address and command and data buffer.

15. The memory component according to claim 9, wherein the compare register generates a test result based on the memory array test data transmitted to the memory array compared with the memory array test data read from the memory array.

16. A method of testing a memory component with built-in self test, comprising:

transmitting input/output test data to an input/output interface having a loopback;

receiving the input/output test data from the loopback of the input/output interface; and

comparing the input/output test data transmitted to the input/output interface with the input/output test data received from the input/output interface.

17. The method according to claim 16, wherein the memory component is a dynamic random access memory (DRAM).

18. The method according to claim 16, wherein the memory component is a buffer.

19. The method according to claim 18, wherein the buffer is an address and command buffer.

20. The method according to claim 18, wherein the buffer is a data buffer.

21. The method according to claim 18, wherein the buffer is an address and command and data buffer.

22. The method according to claim 16, wherein the compare register generates a test result based on the input/output test data transmitted to the input/output interface compared with the input/output test data received from the input/output interface.

23. The method according to claim 16, further including:

transmitting memory array test data to a memory array;

storing the memory array test data in the memory array;

reading the memory array test data from the memory array; and

comparing the memory array test data transmitted to the memory array with the memory array test data read from the memory array.

Sub A4

24. A method of testing a memory component with built-in self test, comprising:

transmitting memory array test data to a memory array;

storing the memory array test data in the memory array

reading the memory array test data from the memory array; and

comparing the memory array test data transmitted to the memory array with the memory array test data read from the memory array.

Sub B1

25. The method according to claim 24, wherein the memory component is a dynamic random access memory (DRAM).

26. The method according to claim 24, wherein the memory component is a buffer.

27. The method according to claim 26, wherein the buffer is an address and command buffer.

28. The method according to claim 26, wherein the buffer is a data buffer.

29. The method according to claim 26, wherein the buffer is an address and command and data buffer.

30. The method according to claim 24, wherein the compare register generates a test result based on the memory array test data transmitted to the memory array compared with the memory array test data read from the memory array.

31. A memory module with built-in self test, comprising:

at least one memory component;

an address and command buffer adapted to transmit address and command data and test data to the at least one memory component, wherein the address and command buffer includes a register to receive a test result; and

at least one data buffer to receive the test data from the address and command buffer, to receive the test data from the at least one memory component, and to compare the test data received from the address and command buffer with the test data received from the at least one memory component to generate the test result.

32. The memory module according to claim 31, wherein the address and command buffer and the data buffer are within a single buffer chip.

33. The memory module according to claim 31, wherein the at least one memory component is a dynamic random access memory (DRAM).

34. The memory module according to claim 31, wherein the address and command buffer includes a clock multiplier to receive a clock signal and to multiply the clock signal for transmission to the at least one memory component and the at least one data buffer.

35. The memory module according to claim 31, wherein the address and command buffer includes an address and command generator to generate the address and command data.

36. The memory module according to claim 31, wherein the test data is obtained from a data bus through a memory controller.

37. The memory module according to claim 31, wherein the register receives the test result from the at least one data buffer and reports the test result as one of the following conditions: built-in self test not enabled, built-in self test enabled, built-in self test failed, and built-in self test passed.

38. The memory module according to claim 31, wherein the at least one data buffer utilizes an exclusive-OR (XOR) comparator to compare the test data received from the address and command buffer with the test data received from the at least one memory component.

39. A method of testing a memory module with built-in self test, the method comprising:

transmitting address and command data and test data to a memory component from an address and command buffer;

receiving the test data from the address and command buffer;

receiving the test data from the memory component; and

comparing the test data received from the address and command buffer with the test data received from the memory component to generate a test result.

40. The method according to claim 39, wherein receiving the test data from the address and command buffer, receiving the test data from the memory component, and comparing the test data are performed in a data buffer.

41. The method according to claim 40, wherein the data buffer and the address and command buffer are within a single buffer chip.

42. The method according to claim 39, wherein the memory component is a dynamic random access memory (DRAM).

43. The method according to claim 39, further including:

receiving a clock signal by a clock multiplier of the address and command buffer;

multiplying the clock signal; and

transmitting the clock signal to the memory component and a data buffer.

44. The method according to claim 39, further including:

generating the address and command data from an address and command data generator of the address and command buffer.

45. The method according to claim 39, further including:

obtaining the test data from a data bus through a memory controller.

46. The method according to claim 39, further including:

receiving the test result in a register of the address and command buffer; and

reporting the test result from the register as one of the following conditions: built-in self test not enabled, built-in self test enabled, built-in self test failed, and built-in self test passed.

47. The method according to claim 39, wherein comparing the test data received from the address and command buffer with the test data received from the memory component is performed by a data buffer utilizing an exclusive-OR (XOR) comparator.

48. A memory module with built-in self test, comprising:

at least one memory component;

an address and command buffer adapted to transmit address and command data and test data to the at least one memory component, wherein the address and command buffer includes,

a register to receive a test result,

a clock multiplier to receive a clock signal and to multiply the clock signal for transmission, and

an address and command generator to generate the address and command data; and

at least one data buffer to receive the test data from the address and command buffer, to receive the test data from the at least one memory component, and to compare the test data received from the address and command buffer with the test data received from the at least one memory component to generate the test result.

49. The memory module according to claim 48, wherein the address and command buffer and the data buffer are within a single buffer chip.

50. The memory module according to claim 48, wherein the at least one memory component is a dynamic random access memory (DRAM).

51. The memory module according to claim 48, wherein the test data is obtained from a data bus through a memory controller.

52. The memory module according to claim 48, wherein the register receives the test result from the at least one data buffer and reports the test result as one of the following conditions: built-in self test not enabled, built-in self test enabled, built-in self test failed, and built-in self test passed.

53. The memory module according to claim 48, wherein the at least one data buffer utilizes an exclusive-OR (XOR) comparator to compare the test data received from the address and command buffer with the test data received from the at least one memory component.